

We claim:

1. In a display system comprising an array of pixel cells formed on a substrate, wherein each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate, a
5 device comprising:

fig 8
a first and second transistor formed on said substrate each having a gate electrode and first and second electrodes defining a serpentine channel region there between, whereby voltage applied to said gate electrode controls conductivity of said channel region.

2. The device of claim 1, wherein a common electrode comprises one of said first and second electrodes of said first transistor and one of said first and second electrodes of said
10 second transistor.

(801)
3. *(21)* The device of claim 1, wherein said first transistor is coupled between a gate line *GL* and a probe pad formed on said substrate and selectively couples said probe pad to said gate line during a test routine whereby charge is written to, stored, and read from said array of pixel cells.

- (801)*
4. The device of claim 1, wherein said first transistor is coupled between a data line and a probe pad formed on said substrate and selectively couples said probe pad to said data line during a test routine whereby charge is written to, stored, and read from said array of pixel cells.
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(803)
5. The device of claim 1, wherein said second transistor is coupled between a gate line and a probe pad formed on said substrate and selectively couples said probe pad to said gate
20 line during a test routine whereby charge is written to, stored, and read from said array of pixel cells.

- (903)*
6. The device of claim 1, wherein said second transistor is coupled between a data line *DL* and a probe pad formed on said substrate and selectively couples said probe pad to said data

[illegible]